CLAIMS

1. A signal processing apparatus employing a second-order Volterra filter for an equalizer configured to equalize an input signal, wherein

a quadratic section of said second-order Volterra filter for implementing a quadratic term of said second-order Volterra filter includes multiplication means for multiplying a first input signal with a second input signal;

said multiplication means including one or more delay means connected in series with one another for delaying a signal output from said multiplication means, each by unit time, coefficient multiplying means for multiplying a signal output from said multiplication means and a signal output from each of said delay means, each with a preset coefficient, and summation means for summing outputs of said coefficient multiplying means together.

2. The signal processing apparatus according to claim 1 wherein said quadratic section includes a plurality of said multiplication means, one of said multiplication means employing a signal not delayed from said first signal, as said second signal, the remaining ones of said multiplication means each employing a signal delayed a preset time from said first signal, as said second signal.

3. The signal processing apparatus according to claim 1 wherein said quadratic section includes n of said multiplication means, n being an integer not less than unity;

a k'th one of said multiplication means, k being an integer such that $1 \leq k \leq n$,

employing a signal corresponding to said first signal delayed by (k−1) times of said unit time as said second signal.

4. A signal processing method employing a second-order Volterra filter for equalizing an input signal, wherein the processing equivalent to a quadratic term of said second-order Volterra filter includes

a multiplication step of multiplying said first signal with said second signal;

a delaying step of delaying a signal, output by said multiplication step, by one or more series-connected delay means, each by a unit time;

a coefficient multiplying step of multiplying a signal output by said multiplication step and a signal output from each of said delaying step, each with a preset coefficient, and a summing step of summing plural outputs of said coefficient multiplying step together.

5. A signal decoding apparatus employing a second-order Volterra filter as an equalizer for equalizing and decoding an input signal, comprising

a linear section of the second-order Volterra filter for implementing a linear term of said second-order Volterra filter and for linear equalization of said input signal;

a quadratic section of the second-order Volterra filter for implementing a quadratic term of said second-order Volterra filter and for non-linear equalization of said input signal;

signal summing means for summing a signal output from said linear section

and a signal output from said quadratic section together; and

most likelihood decoding means for most likelihood decoding a signal output from said signal summing means;

said quadratic section including multiplication means for multiplying a first input signal and a second input signal together;

said multiplication means including one or more series-connected delaying means for delaying signals output from said multiplication means each by a preset unit time, coefficient multiplying means for multiplying a signal output from said multiplication means and a signal output from each of said delaying means, each with a preset coefficient, and summing means for summing outputs of said coefficient multiplying means together.

6. The signal decoding apparatus according to claim 5 wherein said quadratic section includes a plurality of said multiplication means, one of said multiplication means employing a signal not delayed from said first signal, as said second signal, the remaining ones of said multiplication means each employing a signal delayed a preset time from said first signal, as said second signal.

7. The signal decoding apparatus according to claim 5 wherein said quadratic section includes n of said multiplication means, n being an integer not less than unity;

a k'th one of said multiplication means, k being an integer such that $1 \leq k \leq n$, employing a signal corresponding to said first signal delayed by (k−1) times of said

unit time, as said second signal.

8. The signal decoding apparatus according to claim 5 further comprising

error detection means for detecting an error between a signal at each discrete time output from said signal summing means and a target signal;

said coefficient multiplying means updating said preset coefficient every discrete time based on an error detected by said error detection means.

9. A signal decoding method employing a second-order Volterra filter in equalizing and decoding an input signal, comprising

a linear filtering step of implementing the processing equivalent to a linear term of said second-order Volterra filter and linear equalizing said input signal;

a quadratic filtering step of implementing the processing equivalent to a quadratic term of said second-order Volterra filter and non-linear equalizing said input signal;

a signal summing step of summing a signal output from said linear filtering step and a signal output from said quadratic filtering step together; and

a most likelihood decoding step of most likelihood decoding a signal output from said signal summing step;

said quadratic filtering step including

a multiplication step of multiplying said first input signal with said second input signal;

a delaying step of delaying a signal, output by said multiplication step, by

one or more series-connected delay means, each by a unit time;

a coefficient multiplying step of multiplying a signal output by said multiplication step and a signal output from each of said delaying step, each with a preset coefficient; and

a summing step of summing outputs of said coefficient multiplying step together.